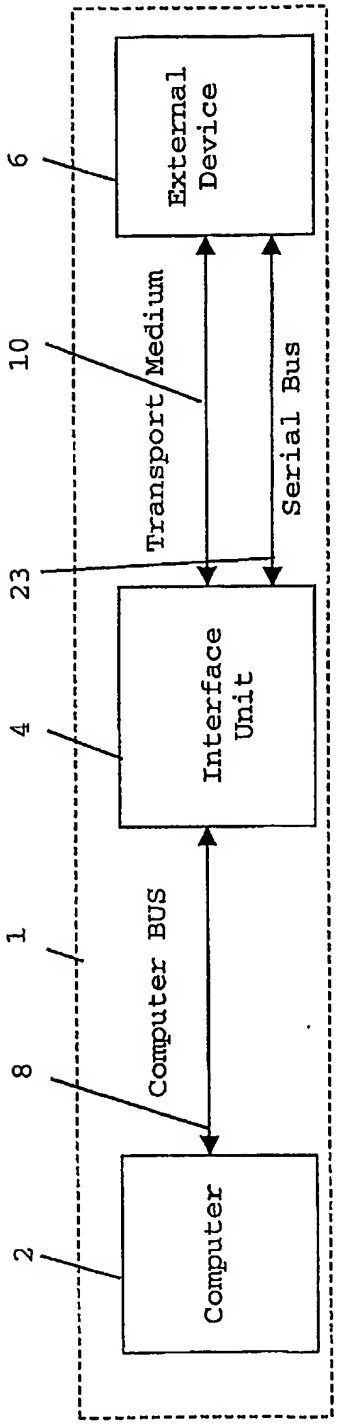

Figure 1

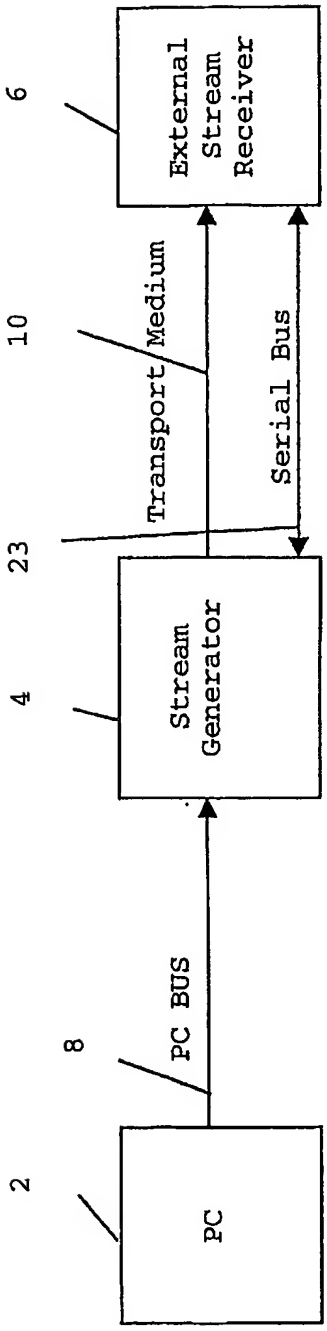

Figure 2

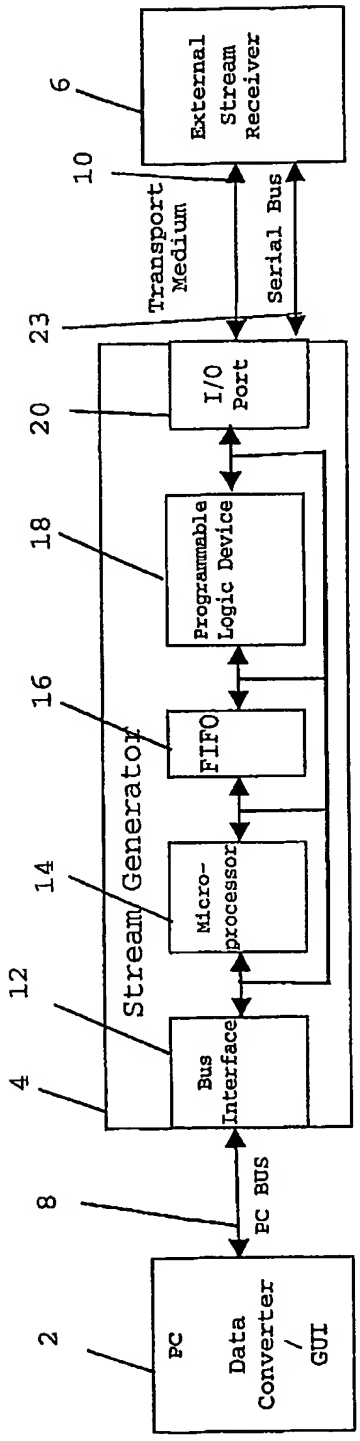

Figure 3

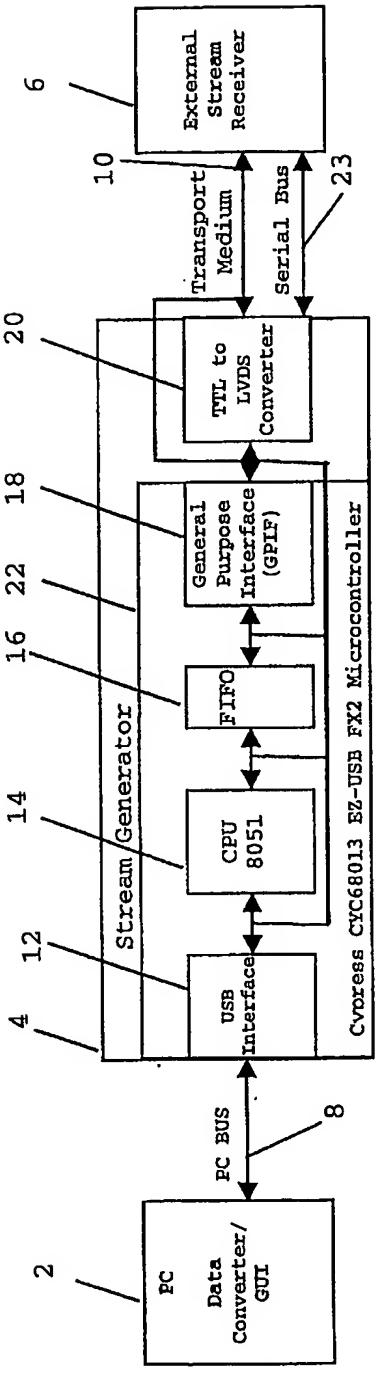

Figure 4

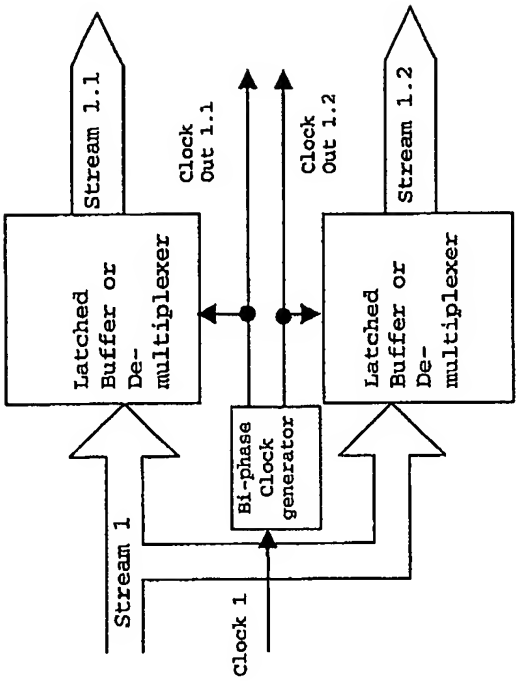

Figure 5 (b)

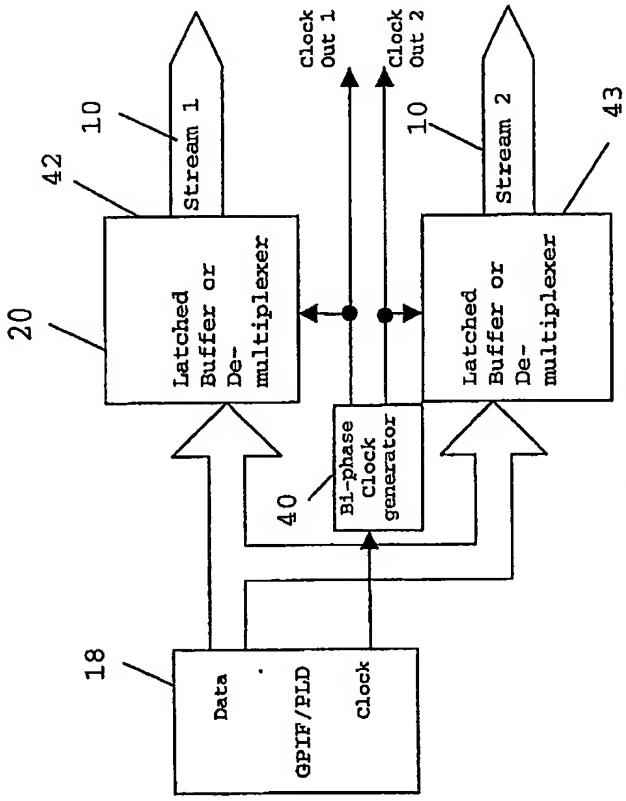

Figure 5(a)

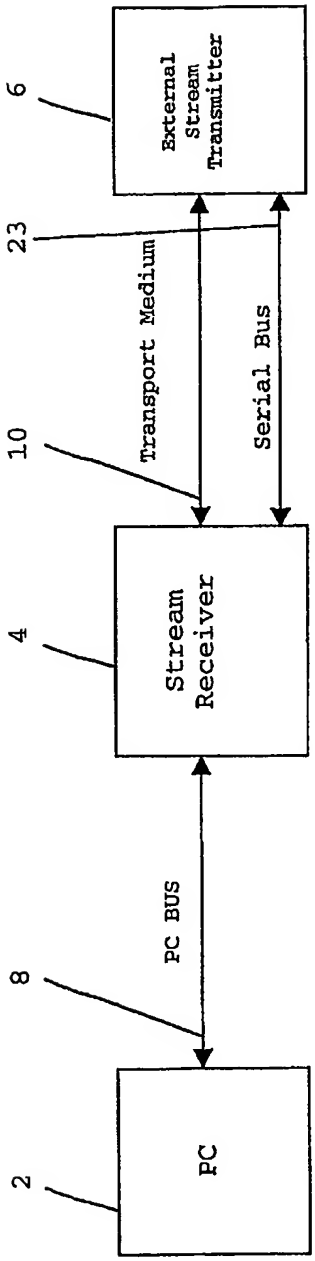

Figure 6

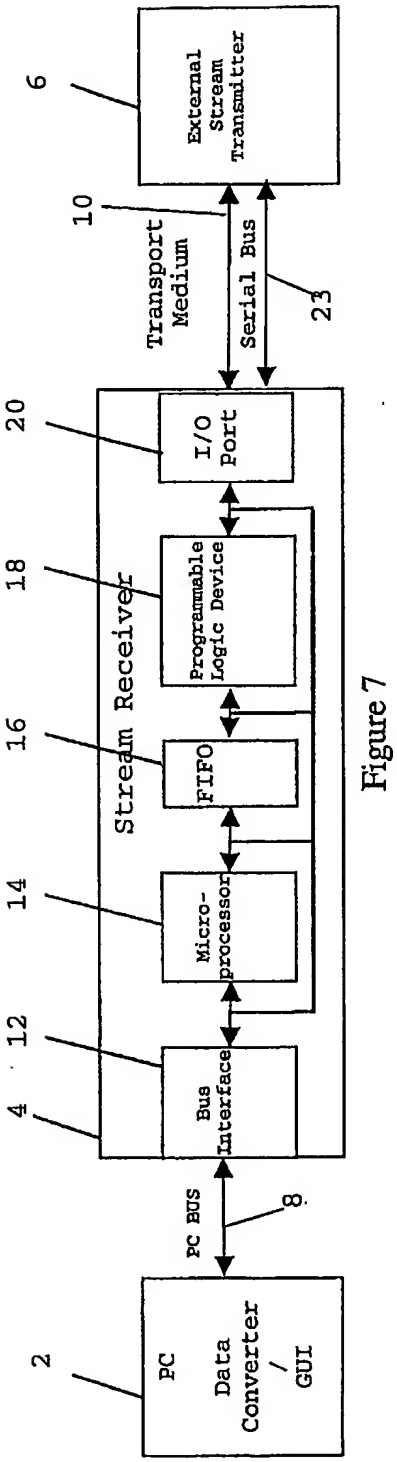

Figure 7

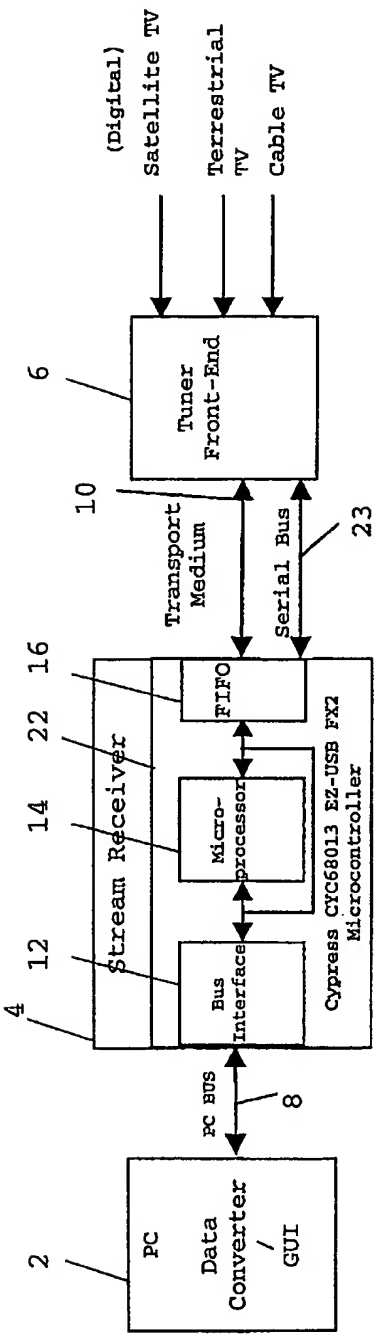

Figure 8

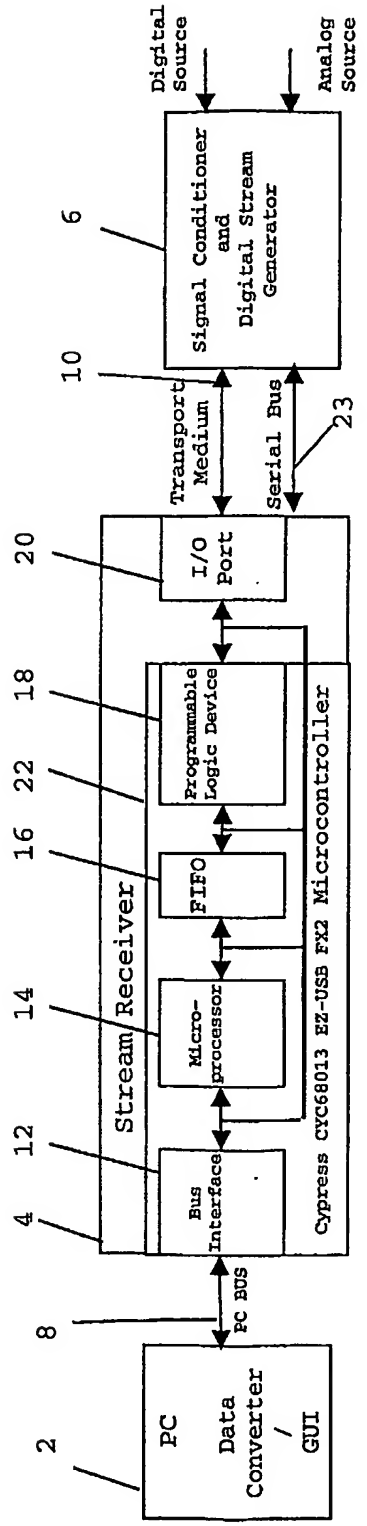

Figure 9

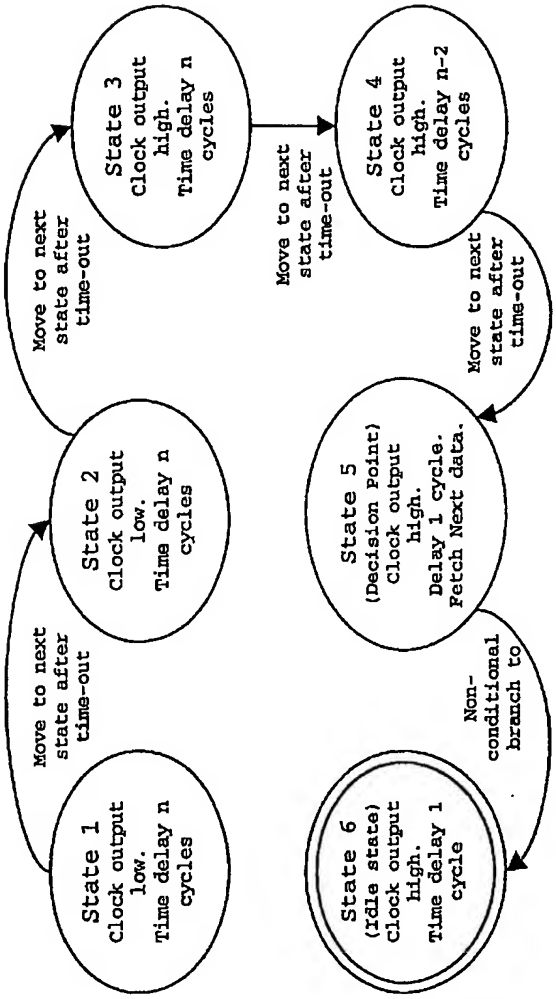
State 1
Clock output low.
Time delay n cycles
Move to next state after time-out
State 2
Clock output low.
Time delay n cycles
Move to next state after time-out
State 3
Clock output high.
Time delay n cycles
Move to next state after time-out
State 4
Clock output high.
Time delay n-2 cycles
Move to next state after time-out
State 5
(Decision Point)
Clock output high.
Delay 1 cycle.
Fetch Next data.
Non-conditional branch to
State 6
(Idle state)
Clock output high.
Time delay 1 cycle

Figure 10.

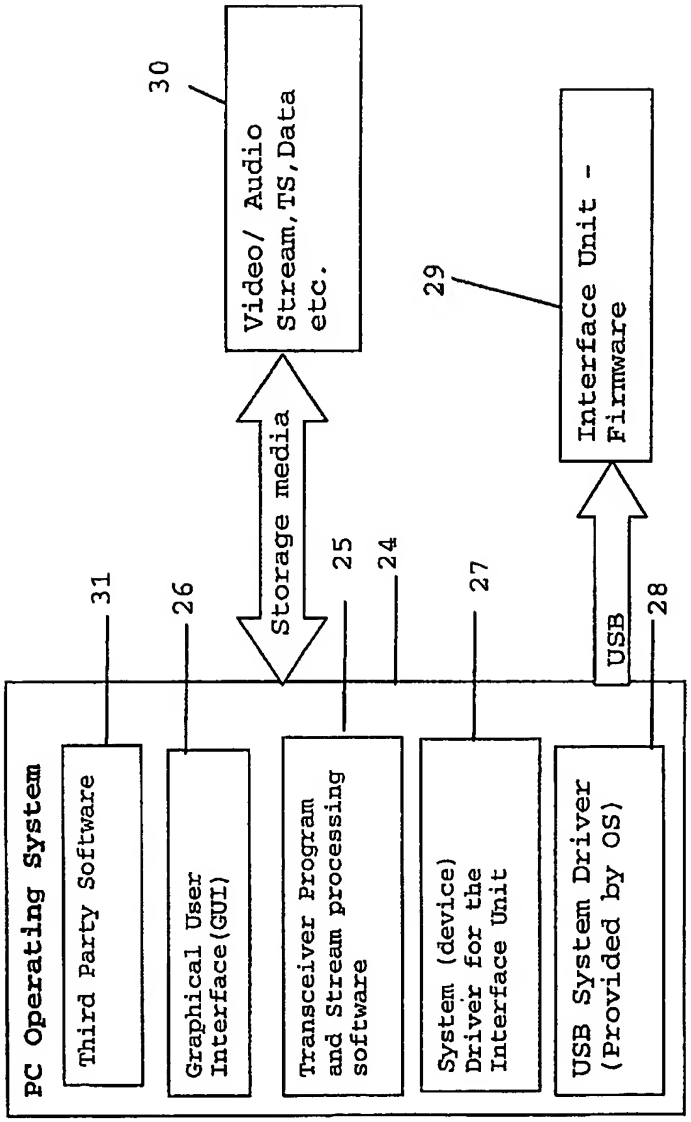
PC Operating System
Third Party Software
Graphical User Interface(GUI)
Transceiver Program and Stream processing software
System (device) Driver for the Interface Unit
USB System Driver (Provided by OS)
USB
Storage media
Video/ Audio Stream,TS,Data etc.
Interface Unit - Firmware
31
26
25
24
27
28
29
30

Figure 11

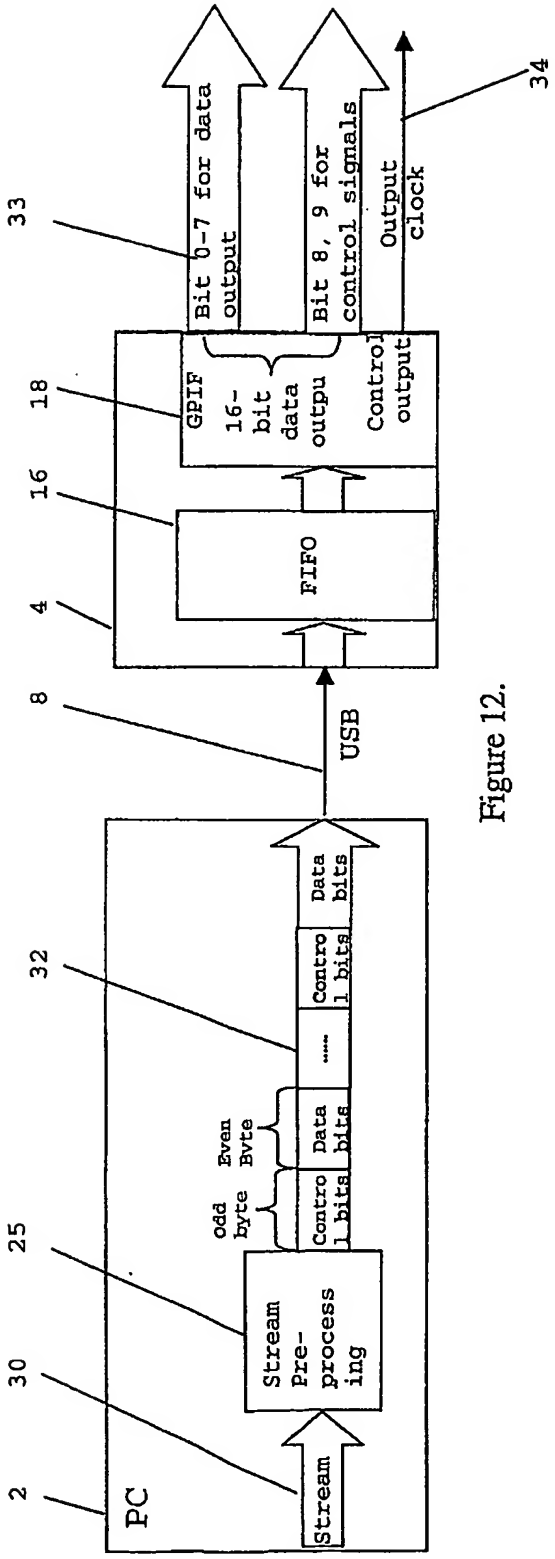
2
PC
Stream
30
25
Stream Pre-process ing
odd byte
Even Byte
Contro l bits
Data bits
.....
Contro l bits
Data bits
32
8
USB
4
16
FIFO
18
GPIF
16-bit data outpu
Control output
33
Bit 0-7 for data output
Bit 8, 9 for control signals
Output clock
34

Figure 12.